CLAIMS

What is claimed is:

1. An amplifier circuit, comprising:

a semiconductor die;

a Doherty amplifier integrated on the semiconductor die, the Doherty amplifier including a peaking amplifier and a carrier amplifier coupled to the peaking amplifier;

a bias circuit integrated on the semiconductor die and coupled to the Doherty amplifier; and

a voltage offset circuit integrated on the semiconductor die and coupled to the bias circuit and to the Doherty amplifier, the voltage offset circuit and the bias circuit together biasing the Doherty amplifier.

2. The amplifier circuit of claim 1, the bias circuit comprising a Field Effect Transistor.

3. The amplifier circuit of claim 1, the voltage offset circuit determining a drive level at which the peaking amplifier is turned to an ON mode.

4. The amplifier circuit of claim 1, further comprising a resistor divider network integrated on the semiconductor die and coupled to the carrier amplifier, the resistor divider network biasing the peaking amplifier.

5. An amplifier circuit, comprising:

a semiconductor die;

at least one amplifier integrated on the semiconductor die;

a bias circuit integrated on the semiconductor die and coupled to the at least one amplifier; and

a voltage offset circuit integrated on the semiconductor die and coupled to the bias circuit and to the at least one amplifier, the voltage offset circuit and the bias circuit together biasing the at least one amplifier.

6. The amplifier circuit of claim 5, the at least one amplifier comprising a peaking amplifier.

7. The amplifier circuit of claim 6, the at least one amplifier comprising a carrier amplifier coupled to the peaking amplifier.

8. The amplifier circuit of claim 5, the bias circuit comprising a Field Effect Transistor.

9. The amplifier circuit of claim 5, the voltage offset circuit determining a drive level at which the at least one amplifier is turned to an ON mode.

10. The amplifier circuit of claim 9, the ON mode comprises operating in a Doherty amplifier configuration.

11. The amplifier circuit of claim 5, the at least one amplifier comprising a peaking amplifier coupled to a carrier amplifier via the voltage offset circuit.

12. The amplifier circuit of claim 11, the bias circuit being coupled to the carrier amplifier.

13. The amplifier circuit of claim 11, further comprising a resistor divide network integrated on the semiconductor die and coupled to the carrier amplifier, the resistor divider network for biasing the peaking amplifier.

14. The amplifier circuit of claim 5, the at least one amplifier comprising a Doherty amplifier.

15. A method, comprising:

providing a semiconductor die having an amplifier integrated on the semiconductor die, a bias circuit integrated on the semiconductor die, and a voltage offset circuit integrated on the semiconductor die;

operating the bias circuit to track device parameters of the amplifier; and

operating the bias circuit and the voltage offset circuit to bias the amplifier based on tracked changes to the device parameters of the amplifier.

16. The method of claim 15, the amplifier comprising a peak amplifier.

17. The method of claim 15, the amplifier comprising a carrier amplifier.

18. The method of claim 15, the bias circuit comprising a Field Effect Transistor.

19. The method of claim 15, the step of tracking device parameters comprising tracking a threshold voltage and transconductance of the amplifier.

20. The method of claim 15, further comprising setting the voltage offset circuitry to a fixed voltage.

21. The method of claim 15, further comprising dynamically adjusting the offset voltage circuitry based on die temperature, process variations, or on load conditions on the at least one amplifier.

22. A method, comprising:

providing a semiconductor die having a first and second amplifier integrated on the semiconductor die, a bias circuit integrated on the semiconductor die, and a voltage offset circuit integrated on the semiconductor die;

operating the bias circuit to provide a reference voltage to the second amplifier; and

operating the voltage offset circuit to automatically bias the first amplifier

proportional to the reference voltage of the second amplifier.

23. The method of claim 22, the first amplifier comprising a peaking amplifier and the second amplifier comprising a carrier amplifier.

24. The method of claim 22, the voltage offset circuit comprising a resistor divider network.